REMARKS

Claims 1-39 remain pending in the current Application. No amendments to the claims are being made herein.

Claim Objections

The Examiner has objected to claims 23 and 24 because they state that the first metal layer includes materials that are compounds. However, as used within the specification and as claimed in claims 23 and 24, the first metal layer is a layer which at least includes a metal, but is not limited to including *only* metal elements. Furthermore, nothing in the application limits the term metal layer to include only metal elements. That is, the first metal layer may be compounds of metal, as claimed in claims 23 and 24 and as provided for in the specification. Therefore, Applicants submit that no correction to claims 23 and 24 is required.

Rejection of claims 1-4 and 26-28

Applicants respectfully submit that claims 1-4 and 26-28 are patentable. The Examiner rejects claim 1 under 35 U.S.C. 102(e) as being anticipated by Chen (US 2004/0198009). Claim 1 states "selectively depositing *a first metal layer on a gate dielectric* of a first region ..." (emphasis added). However, in Chan, the material that is deposited *on* the gate dielectric is polysilicon (layer 46). Even if this polysilicon is considered conductive, the claim specifically claims a metal layer (which must therefore at least include a metal). That is, nothing in Chan teaches or suggests selectively depositing a first metal layer on the gate dielectric. The Examiner states that the combination of polysilicon and silicide form a "conductive layer" and that "this is not excluded by the claims, as claim 27 includes the deposition of polysilicon and metal layers." However, note that in claim 27, a polysilicon layer is formed *over the first metal layer* such that the first metal layer is still between the gate dielectric and the polysilicon layer. That is, this first metal layer, as claimed in claim 1, is still selectively deposited on the gate dielectric, and claim 27 does not change this. Furthermore, in Chan, the silicide is subsequently formed over the polysilicon (i.e. over the gate electrode) and thus not deposited on the gate dielectric. Therefore,

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the Examiner is incorrect in stating that polysilicon layer 46 and/or the silicide teaches or even suggests the first metal layer of claim 1. For at least these reasons, Applcants submit that claim 1 is patentable over Chan.

Claims 2-3 and 26-28 have not been independently addressed since they depend directly or indirectly from allowable claim 1 and are therefore also allowable for at least those reasons provided above with respect to claim 1.

Rejection of claims 23-25 under 35 U.S.C. 103(a)

Claims 23-25 are not being independently addressed since they depend directly or indirectly from allowable claim 1 and are therefore also allowable for at least those reasons provided above with respect to claim 1.

Conclusion

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicants respectfully solicit allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

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